REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended, and in light of the following discussion, is respectfully requested.

Claims 1-7, 9-21, and 25-28 are pending in this application, Claim 8 having been canceled without prejudice or disclaimer; and Claims 25-27 having been presently amended. Support for amended Claims 25-27 can be found, for example, in the original claims, drawings, and specification as originally filed. No new matter has been added.

In the outstanding Office Action, Claims 1-9, 17, 19-21, and 25-28 were rejected under 35 U.S.C. § 103(a) as unpatentable over Aweya et al. (U.S. Patent No. 7,043,651; hereinafter "Aweya") in view of Zdepski et al. (U.S. Patent No. 5,467,137; hereinafter "Zdepski"); and Claims 10-16 and 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski and Lahat et al. (U.S. Patent No. 6,963,561; hereinafter "Lahat").

Applicants acknowledge with appreciation the courtesy of Examiner Findley in granting an interview in this case with Applicants' representative on April 15, 2010, during which time the issues in the outstanding Office Action were discussed as substantially summarized hereinafter and also on the Interview Summary Sheet. No agreement was reached during the interview pending a formal response to the outstanding Office Action.

In response to the rejection of Claims 1-9, 17, 19-21, and 25-28 under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski, Applicants respectfully request reconsideration of the rejection and traverse the rejection as discussed next.

Independent Claim 1 is directed to:

> A method of synchronizing the phase of a local image frame synchronization signal generator of a local video data processor in communication with an asynchronous switched packet network to the phase of a reference image frame synchronization signal generator of a reference video data processor also coupled to said network, said local and reference

> processors having respective clocks, said reference and local image frame synchronization signal generators generating periodic image frame synchronization signals in synchronism with said reference and local clocks respectively, said method comprising the steps of:
>
> ***frequency synchronizing said local and reference clocks***;
>
> said reference video data processor sending, via said network, to said local data processor ***one image timing packet*** providing reference image frame synchronization data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of a reference image frame synchronization signal;
>
> said local video data processor ***controlling the phase of production of said local image frame synchronization signals in dependence on said reference image frame synchronization data and a time of arrival of said one image timing packet***; and
>
> sending to said local video data processor from said reference video data processor, via said network, data packets containing said video data, said image timing packet being sent independently of said data packets.

Independent Claims 25-27 recite substantially similar features as Claim 1. Thus, the arguments presented below with respect to independent Claim 1 are also applicable to independent Claims 25-27.

By way of background, Applicants note that in synchronization systems such as the present invention, reference is made to local and reference clocks; these are the master sources of system timekeeping within the local and reference devices respectively, and a lot of effort is put into ensuring that the frequency of the local clock (and hence its timekeeping) is kept as close as possible to that of the reference clock. This activity is recited within claim 1 in the method step of "frequency synchronizing said local and reference clocks." As discussed below, these are the clocks mentioned in Awaya and Zdepski. However, over and

above this activity, Claim 1 further recites phase synchronization of image frame synchronization signals. This additional operation is not described by either Awaya or Zdepski, as detailed below.

Regarding Awaya, Applicants first note that Awaya describes that the timestamps are embedded in data packets.[1] Also, the cited passage in the Office Action at col. 3 lines 17-20 of Awaya refers to prior art in the background section, which is taught to be inferior. Thus Awaya teaches away from using Applicants' approach. In any event, the timestamps in Awaya clearly relate to the frequency synchronization of system clocks (see col. 1, lines 21-24 and 33-36; col. 3 lines 54-57; and col. 8 lines 46-53 of Awaya). Notably, the timestamps described in Awaya (both in the background section and in the description of the device in Awaya) are used solely for the purpose of synchronizing these system clocks. However, there is no mention of frame count phase synchronization whatsoever.

Turning now to Zdepski, Applicants note that the cited passage in the Office Action at col. 3 lines 12-23 of Zdepski specifically describes that frame counts (PTRs) are "included in the compressed video signal stream' (line 15), whilst in contrast, program clock references or PCRs are 'embedded as auxiliary data ...[in]... auxiliary transport packets." Thus, Zdepski clearly and explicitly differentiates between frame counts (PTRs) and timestamps/clock references (PCRs), and equally explicitly teaches that frame counts (PTRs) are embedded in data and ***not*** in auxiliary packets (contrary to Applicants' claimed invention), while timestamp /clock references (PCRs) ***are*** embedded in auxiliary packets. Further as noted above, Awaya describes that embedding clock references in auxiliary packets is an inferior approach and that they should also be embedded in data packets.

As a result, the only conclusion that a person of ordinary skill in the art can reach from the combined teachings of Awaya and Zdepski is that timestamps/clock references

[1] See column 12, lines 18-26 of Awaya.

(PCRs) should join frame counts (PTRs) within the data packets. To conclude otherwise specifically overturns the teachings of Awaya and Zdepski and clearly requires the benefit of hindsight given by the present invention. Thus, Applicants respectfully traverse the Office Action's conclusion at point 3 on page 3 of the Office Action and conclude that the only technically sensible interpretation of the cited references is to teach that frame counts are part of data packets. Further, the PCR in Zdepski is used to correct the local system clock frequency in a similar manner to the timestamps in Awaya described at column 4, line 50 to column 5, line 7. However, in Zdepski, PTRs are not mentioned again in reference to ***any*** form of synchronization, including PTR phase synchronization.

Thus, in summary, Awaya and Zdepski in combination would teach a person of ordinary skill in the art to embed timestamps within data packets, and use these timestamps to synchronize the frequency of a local system clock to a reference system clock. Meanwhile Zdepski also explicitly describes that frame counts are also embedded within data packets. Neither document describes ***additional*** processes over and above frequency synchronization of the local and reference clocks relating to the synchronization of frame counts, and in particular synchronizing the ***phase*** of frame counts.

By contrast this is precisely what Applicants' Claim 1 recites, the frequency synchronization of the local and reference clocks (the subject of Awaya and Zdepski) is merely the first step in the Applicants' claimed method. Subsequently, additional steps are recited that relate to an "image timing packet" that includes an "image frame synchronization signal" for the purpose of "synchronizing the phase of the local image frame synchronization signal generator."

Applicants also respectfully traverse the assertions at point 4 of the Response to Arguments section at page 2 of the Office Action, as none of the terms "image timing packet," "image frame synchronization signal," or "synchronizing the phase of the local

image frame synchronization signal generator" relate to synchronization of a system clock, and Applicants note that it is clear from the claim that these are additional steps beyond the recited step of "frequency synchronizing said local and reference clocks" in the claims.

Thus, Applicants respectfully submit that independent Claims 1 and 25-27 (and all claims depending thereon) patentably distinguish over Awaya and Zdepski either alone or in proper combination.

Accordingly, Applicants respectfully request that the rejection of Claims 1-9, 17, 19-21, and 25-28 under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski, be withdrawn.

In response to the rejection of Claims 10-16 and 18 under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski and Lahat, Applicants note that Claims 10-16 and 18 are dependent on Claim 1 and are thus believed to be patentable for at least the reasons described above. Further, Applicants respectfully submit that Lahat fails to cure any of the above-noted deficiencies of Awaya and Zdepski.

Consequently, in view of the present amendment, and in light of the above discussion, the pending claims as presented herewith are believed to be in condition for formal allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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